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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,125	06/29/2001	Shunpei Yamazaki	740756-2330	7248

31780 7590 12/15/2006

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,125	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17,19-30 and 47-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,19-30 and 47-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-17, 19-30, and 47-64 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-26 of U.S. Patent No. 7,084,016.

Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons:

The claimed subject matter of the instant application as claimed in claims 1-17, 19-30, and 47-64 is essentially claimed in claims 1-26 of U.S. Patent No. 7,084,016. The scope of the instant application claimed invention is similar to that of the scope of U.S. Patent No. 7,084,016 and conflicting claims are not patentably distinct from each other.

3. Claim 1-17, 19-30, and 47-64 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-36 of copending Application No. 11/266,369.

Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons:

The claimed subject matter of the instant application as claimed in claims 1-17, 19-30, and 47-64 is essentially claimed in claims 1-36 of U.S. copending Application No. 11/266,369. The scope of the instant application claimed invention is similar to that of the scope of U.S. copending Application No. 11/266,369and conflicting claims are not patentably distinct from each other.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 19, 20, 23-30, 47, 48 and 51-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morosawa (JP/07038113) in view of Hara et al. (US/5,648,276).

The rejection that was mailed on June 26, 2006 is maintained and repeated herein below as of record.

Re claim 19, 25, 27 and 29, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate; irradiating said semiconductor film with laser light in an atmosphere containing oxygen for crystallizing said semiconductor film; removing an oxide film formed on a surface of the semiconductor film by etching with buffered HF (i.e., 1% HF) after the first irradiation of the laser light and before the second laser light irradiation; and leveling the surface of the crystallized semiconductor film by heating in an atmosphere containing in inert gas or oxygen or the combination of after removing the oxide film, in an atmosphere containing predetermined concentration of oxygen or an oxygen compound (see the English translation that was submitted by Applicants on April 18, 2005).

However, Morosawa does not specifically disclose recrystallizing the crystallized semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the

surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Both Morosawa and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

However, both Morosawa and Hara et al. silent about the concentration of oxygen or oxygen compound being 10 ppm or less during the leveling step. Although the concentration is not specifically disclosed by Morosawa and Kudo et al., such oxygen concentration rage can be set within the level ordinary skill in the art by routine optimization to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

One of ordinary skill in would have motivated to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine

experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed concentration range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claims 20, 26, 28, and 30, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate; irradiating the semiconductor film with laser light in an atmosphere containing oxygen for crystallizing said semiconductor film; treating a surface of the semiconductor film with a buffered hydrofluoric acid (i.e., 1% HF) after the first irradiation of the laser light before the second irradiation of light; and leveling the surface of the semiconductor film by heating after the treatment with the hydrofluoric acid in an atmosphere, in an atmosphere containing predetermined concentration of oxygen or an oxygen compound (see the English translation that was submitted by Applicants on April 18, 2005).

However, Morosawa does not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and

recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Both Morosawa and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

However, both Morosawa and Hara et al. silent about the concentration of oxygen of oxygen compound being 10 ppm or less during the leveling step. Although the concentration is not specifically disclosed by Morosawa and Kudo et al., such oxygen concentration rage can be set within the level ordinary skill in the art by routine optimization to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

One of ordinary skill in would have motivated to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide, since it has been held where the general conditions of a claim are disclosed in the

prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed concentration range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 23, as applied to claim 19 above, Morosawa and Hara et al. in combination disclose all the claimed limitations including leveling (i.e., annealing) the semiconductor film at temperature between 500 and 600 °C (i.e., outside the claimed temperature range of 900 and 1200 °C) (see the English translation that was submitted by Applicants on April 18, 2005).

One of ordinary skill in the art would have been motivated to optimize the claimed annealing temperature range by using routine experimentation in order to achieve the desired device performance.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the claimed annealing temperature range, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843

(Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed temperature range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 24, as applied to claim 20 above, Morosawa and Hara et al. in combination disclose all the claimed limitations including leveling (i.e., annealing) the semiconductor film at temperature between 500 and 600 °C (i.e., outside the claimed temperature range of 900 and 1200 °C) (see the English translation that was submitted by Applicants on April 18, 2005).

One of ordinary skill in the art would have been motivated to optimize the claimed annealing temperature range by using routine experimentation in order to achieve the desired device performance.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the claimed annealing temperature range, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed

temperature range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claims 47, 53, 55, and 57, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon (2 3) over a substrate (see Drawing 1, Examples and Abstract); irradiating the semiconductor film with laser light in an atmosphere containing oxygen for crystallizing said semiconductor film (see Examples Paragraph 0009); removing a natural oxidation film (8) formed on a surface of the semiconductor film by etching (i.e., dipping in 1% HF solution) after the first irradiation of the laser light and before the second radiation anneal treatment; and leveling the surface of the semiconductor film by heating in the atmosphere containing inert gas in reducing atmosphere (i.e., in treating the film with NH_3 and N_2 plasma ; see page 6/10 and lines 5-17 of the English translation that was submitted by Applicants on April 18, 2005) after removing the natural oxidation film (see the English translation that was submitted by Applicants on April 18, 2005).

However, Morosawa does not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Both Morosawa and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

Re claims 48, 54, 56, and 58, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate; irradiating the semiconductor film with laser light in an atmosphere containing oxygen for crystallizing the semiconductor film; treating a surface of the semiconductor film with a hydrofluoric acid to remove a natural oxidation film formed on the surface of the semiconductor film after the irradiation of the laser light; and leveling the surface of the semiconductor film by heating in inert gate (i.e., nitrogen gas) or in reducing atmosphere (i.e., in hydrogen) after the treatment with the hydrofluoric acid i.e., dipping in 1% HF solution) before the second radiation anneal treatment (see the English translation that was submitted by Applicants on April 18, 2005).

However, Morosawa does not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and

recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Both Morosawa and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

Re claim 51, as applied to claim 47 above, Morosawa and Hara et al. in combination disclose all the claimed limitations including leveling (i.e., annealing) the semiconductor film at temperature between 500 and 600 °C (i.e., outside the claimed temperature range of 900 and 1200 °C) (see the English translation Examples in Paragraph 0010).

One of ordinary skill in the art would have been motivated to optimize the claimed annealing temperature range by using routine experimentation in order to achieve the desired device performance.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the claimed annealing temperature range, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809

(CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed temperature range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 52, as applied to claim 47 above, Morosawa and Hara et al. in combination disclose all the claimed limitations including leveling (i.e., annealing) the semiconductor film at temperature between 500 and 600 °C (i.e., outside the claimed temperature range of 900 and 1200 °C) (see the English translation that was submitted by Applicants on April 18, 2005).

With respect to the temperature range, one of ordinary skill in the art would have been motivated to optimize the claimed annealing temperature range by using routine experimentation in order to achieve the desired device performance.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the claimed annealing temperature range, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997).

Furthermore, the specification contains no disclosure of either the critical nature of the claimed temperature range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

6. Claims 21, 22, 49 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morosawa (JP/07038113) and Hara et al. (US/5,648,276), and further in view of Yamazaki et al. (US/5,608,232).

The rejection that was mailed on June 26, 2006 is maintained and repeated herein below as of record.

Re claim 21, as applied to claim 19 in Paragraph 5 above, Morosawa Hara et al. in combination disclose all the claimed limitations including annealing of the substrate during the leveling step.

However, Morosawa and Hara et al. do not specifically disclose furnace annealing.

Yamazaki et al. disclose furnace annealing of the substrate in nitrogen atmosphere in order to crystallize the semiconductor layer (see Yamazaki et al. Col. 24, lines 10-30).

Morosawa, Hara et al. and Yamazaki et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Hara et al. and Yamazaki et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Hara et al. reference with

furnace annealing during leveling process of the semiconductor layer as taught by Yamazaki et al. in order to crystallize the semiconductor layer.

Re claim 22, as applied to claim 20 in Paragraph 5 above, Morosawa and Hara et al. disclose all the claimed limitations including annealing of the substrate during the leveling step.

However, Morosawa and Hara et al. do not specifically disclose furnace annealing.

Yamazaki et al. disclose furnace annealing of the substrate in nitrogen atmosphere in order to crystallize the semiconductor layer (see Yamazaki et al. Col. 24, lines 10-30).

Both Morosawa, Hara et al. and Yamazaki et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Hara et al. and Yamazaki et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Hara et al. reference with furnace annealing during leveling process of the semiconductor layer as taught by Yamazaki et al. in order to crystallize the semiconductor layer.

Re claim 49, as applied to claim 47 in Paragraph 2 above, Morosawa and Hara et al. in combination disclose all the claimed limitations including annealing of the substrate during the leveling step.

However, Morosawa and Hara et al. do not specifically disclose furnace annealing.

Yamazaki et al. disclose furnace annealing of the substrate in nitrogen atmosphere in order to crystallize the semiconductor layer (see Yamazaki et al. Col. 24, lines 10-30).

Morosawa, Hara et al. and Yamazaki et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin

film the crystallize the thin film. Therefore, the teachings of Morosawa, Hara et al. and Yamazaki et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Hara et al. reference with furnace annealing during leveling process of the semiconductor layer as taught by Yamazaki et al. in order to crystallize the semiconductor layer.

Re claim 50, as applied to claim 48 in Paragraph 5 above, Morosawa and Hara et al. in combination disclose all the claimed limitations including annealing of the substrate during the leveling step.

However, Morosawa and Hara et al. do not specifically disclose furnace annealing.

Yamazaki et al. disclose furnace annealing of the substrate in nitrogen atmosphere in order to crystallize the semiconductor layer (see Yamazaki et al. Col. 24, lines 10-30).

Morosawa, Hara et al. and Yamazaki et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Hara et al. and Yamazaki et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Hara et al. reference with furnace annealing during leveling process of the semiconductor layer as taught by Yamazaki et al. in order to crystallize the semiconductor layer.

7. Claims 1-12, 14-17, 59, and 61-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morosawa (JP/07038113) in view of Kudo et al. (JP/09186336), and further in view of Hara et al. (US/5,648,276).

The rejection that was mailed on June 26, 2006 is maintained and repeated herein below as of record.

Re claim 1, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon (2 or 3) (see Drawing 1 and Examples and Abstract) over a substrate (1); irradiating the semiconductor film with laser light for crystallizing the semiconductor film (see Examples Paragraph 0009); removing a natural oxidation film (8) (see Drawing 7 and 8; Examples, Paragraph 0010) formed on a surface of the semiconductor film by etching after the irradiation of the laser light (i.e., by dipping in HF); and leveling the surface of the crystallized semiconductor film by heating after removing the natural oxidation film (see the English translation that was submitted by Applicants on April 18, 2005).

Although Morosawa discloses irradiating said semiconductor film (i.e., an amorphous silicon film) with a leaser light for crystallizing the semiconductor film, Morosawa is silent about irradiating the semiconductor film with leaser light in air.

Kudo et al. disclose method of manufacturing thin film transistor the method includes depositing an amorphous silicon film (25) (i.e., a semiconductor layer) and irradiating the amorphous silicon film (25) with an excimer laser in atmosphere containing an air in order to dehydrogenate the amorphous silicon film and change into polysilicon thin film (see Abstract and Drawing 2).

Both Morosawa and Kudo et al. teachings directed to irradiating amorphous thin film layer using laser light to crystallize the thin film after the thin film deposited for fabrication of TFTs. Therefore, the teachings of Morosawa and Kudo et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with irradiating on

the semiconductor film (i.e., amorphous silicon film) in air as taught by Kudo et al. in order to dehydrogenate the amorphous silicon film and convert it to polysilicon thin film.

However, both Morosawa and Kudo et al. do not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Morosawa, Kudo et al. and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al. and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Kudo et al. reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

Re claims 2, 16, and 17, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate; irradiating said semiconductor film with laser light for crystallizing the semiconductor film; removing an oxide film formed on a surface of the semiconductor film by

etching (i.e., treating) the surface with buffered HF (i.e., 1% HF) after the irradiation of the laser light; and leveling the surface of the crystallized semiconductor film by heating in a reducing atmosphere containing hydrogen after removing the oxide film (see the English translation Example in Paragraph 0007 through Paragraph 00016).

Although Morosawa discloses irradiating said semiconductor film (i.e., an amorphous silicon film) with a leaser light for crystallizing the semiconductor film, Morosawa is silent about irradiating the semiconductor film with leaser light in air.

Kudo et al. disclose method of manufacturing thin film transistor the method includes depositing an amorphous silicon film (25) (i.e., a semiconductor layer) and irradiating the amorphous silicon film (25) with an excimer laser in atmosphere containing an air in order to dehydrogenate the amorphous silicon film and change into polysilicon thin film (see Abstract and Drawing 2).

Both Morosawa and Kudo et al. teachings directed to irradiating amorphous thin film layer using laser light to crystallize the thin film after the thin film deposited for fabrication of TFTs. Therefore, the teachings of Morosawa and Kudo et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with irradiating on the semiconductor film (i.e., amorphous silicon film) in air as taught by Kudo et al. in order to dehydrogenate the amorphous silicon film and convert it to polysilicon thin film.

However, both Morosawa and Kudo et al. do not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and

crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Morosawa, Kudo et al. and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al. and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Kudo et al. reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

Re claims 3 and 15, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate; irradiating the semiconductor film with laser light for crystallizing said semiconductor film; removing an oxide film formed on a surface of the semiconductor film by etching after the irradiation of the laser light; and leveling the surface of the crystallized semiconductor film by heating in an inert gas (i.e., nitrogen) after removing said oxide film (see the English translation that was submitted by Applicants on April 18, 2005).

Although Morosawa discloses irradiating said semiconductor film (i.e., an amorphous silicon film) with a leaser light for crystallizing the semiconductor film, Morosawa is silent about irradiating the semiconductor film with leaser light in air.

Kudo et al. disclose method of manufacturing thin film transistor the method includes depositing an amorphous silicon film (25) (i.e., a semiconductor layer) and irradiating the amorphous silicon film (25) with an excimer laser in atmosphere containing an air in order to dehydrogenate the amorphous silicon film and change into polysilicon thin film (see Abstract and Drawing 2).

Both Morosawa and Kudo et al. teachings directed to irradiating amorphous thin film layer using laser light to crystallize the thin film after the thin film deposited for fabrication of TFTs. Therefore, the teachings of Morosawa and Kudo et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with irradiating on the semiconductor film (i.e., amorphous silicon film) in air as taught by Kudo et al. in order to dehydrogenate the amorphous silicon film and convert it to polysilicon thin film.

However, both Morosawa and Kudo et al. do not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Morosawa, Kudo et al. and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin

film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al. and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Kudo et al. reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

Re claim 4, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate; irradiating said semiconductor film with laser light for crystallizing said semiconductor film; removing an oxide film formed on a surface of the semiconductor film by etching after the irradiation of the laser light; and leveling the surface of the crystallized semiconductor film by heating in an atmosphere after removing the oxide film, in an atmosphere containing predetermined concentration of oxygen or an oxygen compound (see the English translation that was submitted by Applicants on April 18, 2005).

Although Morosawa discloses irradiating said semiconductor film (i.e., an amorphous silicon film) with a leaser light for crystallizing the semiconductor film, Morosawa is silent about irradiating the semiconductor film with leaser light in air and the concentration of oxygen or oxygen compound being 10 ppm or less.

Kudo et al. disclose method of manufacturing thin film transistor the method includes depositing an amorphous silicon film (25) (i.e., a semiconductor layer) and irradiating the amorphous silicon film (25) with an excimer laser in atmosphere containing an air in order to

dehydrogenate the amorphous silicon film and change into polysilicon thin film (see Abstract and Drawing 2).

Both Morosawa and Kudo et al. teachings directed to irradiating amorphous thin film layer using laser light to crystallize the thin film after the thin film deposited for fabrication of TFTs. Therefore, the teachings of Morosawa and Kudo et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with irradiating on the semiconductor film (i.e., amorphous silicon film) in air as taught by Kudo et al. in order to dehydrogenate the amorphous silicon film and convert it to polysilicon thin film.

However, both Morosawa and Kudo et al. do not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Morosawa, Kudo et al. and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al. and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Kudo et al. reference with

recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

However, the combination of Morosawa, Kudo et al. and Hara et al. is silent about the concentration of oxygen of oxygen compound being 10 ppm or less during the leveling step. Although the concentration is not specifically disclosed by Morosawa and Kudo et al., such oxygen concentration rage can be set within the level ordinary skill in the art by routine optimization to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

One of ordinary skill in would have motivated to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed concentration range or any unexpected results arising

therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 5, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate; irradiating said semiconductor film with laser light in air for crystallizing said semiconductor film; removing an oxide film formed on a surface of the semiconductor film by etching after the irradiation of the laser light; and leveling the surface of the semiconductor film by heating in a reducing atmosphere after removing said oxide film, a concentration of oxygen or an oxygen compound contained in said reducing atmosphere, in an atmosphere containing predetermined concentration of oxygen or an oxygen compound (see the English translation that was submitted by Applicants on April 18, 2005).

Although Morosawa discloses irradiating said semiconductor film (i.e., an amorphous silicon film) with a leaser light for crystallizing the semiconductor film, Morosawa is silent about irradiating the semiconductor film with leaser light in air and the concentration of oxygen or oxygen compound being 10 ppm or less.

Kudo et al. disclose method of manufacturing thin film transistor the method includes depositing an amorphous silicon film (25) (i.e., a semiconductor layer) and irradiating the amorphous silicon film (25) with an excimer laser in atmosphere containing an air in order to dehydrogenate the amorphous silicon film and change into polysilicon thin film (see Abstract and Drawing 2).

Both Morosawa and Kudo et al. teachings directed to irradiating amorphous thin film layer using laser light to crystallize the thin film after the thin film deposited for fabrication of TFTs. Therefore, the teachings of Morosawa and Kudo et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with irradiating on the semiconductor film (i.e., amorphous silicon film) in air as taught by Kudo et al. in order to dehydrogenate the amorphous silicon film and convert it to polysilicon thin film.

However, both Morosawa and Kudo et al. do not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Morosawa, Kudo et al. and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al. and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Kudo et al. reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide

removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

However, the combination of Morosawa, Kudo et al. and Hara et al. is silent about the concentration of oxygen of oxygen compound being 10 ppm or less during the leveling step. Although the concentration is not specifically disclosed by Morosawa and Kudo et al., such oxygen concentration rage can be set within the level ordinary skill in the art by routine optimization to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

One of ordinary skill in would have motivated to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed concentration range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon

another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 6, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate; irradiating said semiconductor film with laser light for crystallizing said semiconductor film; removing an oxide film formed on a surface of the semiconductor film by etching after the irradiation of the laser light; and leveling the surface of the crystallized semiconductor film by heating in an inert gas after removing said oxide film, in an atmosphere containing predetermined concentration of oxygen or an oxygen compound (see the English translation that was submitted by Applicants on April 18, 2005).

Although Morosawa discloses irradiating said semiconductor film (i.e., an amorphous silicon film) with a leaser light for crystallizing the semiconductor film, Morosawa is silent about irradiating the semiconductor film with leaser light in air and the concentration of oxygen or oxygen compound being 10 ppm or less.

Kudo et al. disclose method of manufacturing thin film transistor the method includes depositing an amorphous silicon film (25) (i.e., a semiconductor layer) and irradiating the amorphous silicon film (25) with an excimer laser in atmosphere containing an air in order to dehydrogenate the amorphous silicon film and change into polysilicon thin film (see Abstract and Drawing 2).

Both Morosawa and Kudo et al. teachings directed to irradiating amorphous thin film layer using laser light to crystallize the thin film after the thin film deposited for fabrication of TFTs. Therefore, the teachings of Morosawa and Kudo et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with irradiating on the semiconductor film (i.e., amorphous silicon film) in air as taught by Kudo et al. in order to dehydrogenate the amorphous silicon film and convert it to polysilicon thin film.

However, both Morosawa and Kudo et al. do not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Morosawa, Kudo et al. and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al. and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Kudo et al. reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

However, the combination of Morosawa, Kudo et al. and Hara et al. is silent about the concentration of oxygen of oxygen compound being 10 ppm or less during the leveling step.

Although the concentration is not specifically disclosed by Morosawa and Kudo et al., such oxygen concentration rage can be set within the level ordinary skill in the art by routine optimization to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

One of ordinary skill in would have motivated to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed concentration range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 7, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate;

irradiating said semiconductor film with laser light for crystallizing the semiconductor film; treating a surface of the semiconductor film with a hydrofluoric acid to remove a natural oxidation film formed on the surface of the semiconductor film after the irradiation of the laser light; and leveling the surface of the crystallized semiconductor film by heating after the treatment with the hydrofluoric acid (see the English translation Example in Paragraph 0007 through Paragraph 00016).

Although Morosawa discloses irradiating said semiconductor film (i.e., an amorphous silicon film) with a leaser light for crystallizing the semiconductor film, Morosawa is silent about irradiating the semiconductor film with leaser light in air.

Kudo et al. disclose method of manufacturing thin film transistor the method includes depositing an amorphous silicon film (25) (i.e., a semiconductor layer) and irradiating the amorphous silicon film (25) with an excimer laser in atmosphere containing an air in order to dehydrogenate the amorphous silicon film and change into polysilicon thin film (see Abstract and Drawing 2).

Both Morosawa and Kudo et al. teachings directed to irradiating amorphous thin film layer using laser light to crystallize the thin film after the thin film deposited for fabrication of TFTs. Therefore, the teachings of Morosawa and Kudo et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with irradiating on the semiconductor film (i.e., amorphous silicon film) in air as taught by Kudo et al. in order to dehydrogenate the amorphous silicon film and convert it to polysilicon thin film.

However, both Morosawa and Kudo et al. do not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Morosawa, Kudo et al. and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al. and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Kudo et al. reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

Re claim 8, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate; irradiating the semiconductor film with laser light for crystallizing the semiconductor film; treating a surface of the semiconductor film with a hydrofluoric acid after the irradiation of the laser light; and leveling the surface of the semiconductor film by heating after the treatment with the hydrofluoric acid in a reducing atmosphere (see the English translation Example in Paragraph 0007 through Paragraph 00016).

Although Morosawa discloses irradiating said semiconductor film (i.e., an amorphous silicon film) with a leaser light for crystallizing the semiconductor film, Morosawa is silent about irradiating the semiconductor film with leaser light in air.

Kudo et al. disclose method of manufacturing thin film transistor the method includes depositing an amorphous silicon film (25) (i.e., a semiconductor layer) and irradiating the amorphous silicon film (25) with an excimer laser in atmosphere containing an air in order to dehydrogenate the amorphous silicon film and change into polysilicon thin film (see Abstract and Drawing 2).

Both Morosawa and Kudo et al. teachings directed to irradiating amorphous thin film layer using laser light to crystallize the thin film after the thin film deposited for fabrication of TFTs. Therefore, the teachings of Morosawa and Kudo et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with irradiating on the semiconductor film (i.e., amorphous silicon film) in air as taught by Kudo et al. in order to dehydrogenate the amorphous silicon film and convert it to polysilicon thin film.

However, both Morosawa and Kudo et al. do not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Morosawa, Kudo et al. and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al. and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Kudo et al. reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

Re claim 9, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate; irradiating the semiconductor film with laser light for crystallizing said semiconductor film; treating a surface of the semiconductor film with a hydrofluoric acid after the irradiation of the laser light; and leveling the surface of the crystallized semiconductor film by heating after the treatment with the hydrofluoric acid in an inert gas (see the English translation Example in Paragraph 0007 through Paragraph 00016).

Although Morosawa discloses irradiating said semiconductor film (i.e., an amorphous silicon film) with a leaser light for crystallizing the semiconductor film, Morosawa is silent about irradiating the semiconductor film with leaser light in air.

Kudo et al. disclose method of manufacturing thin film transistor the method includes depositing an amorphous silicon film (25) (i.e., a semiconductor layer) and irradiating the amorphous silicon film (25) with an excimer laser in atmosphere containing an air in order to

dehydrogenate the amorphous silicon film and change into polysilicon thin film (see Abstract and Drawing 2).

Both Morosawa and Kudo et al. teachings directed to irradiating amorphous thin film layer using laser light to crystallize the thin film after the thin film deposited for fabrication of TFTs. Therefore, the teachings of Morosawa and Kudo et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with irradiating on the semiconductor film (i.e., amorphous silicon film) in air as taught by Kudo et al. in order to dehydrogenate the amorphous silicon film and convert it to polysilicon thin film.

However, both Morosawa and Kudo et al. do not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Morosawa, Kudo et al. and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al. and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Kudo et al. reference with

recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

Re claim 10, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate; irradiating said semiconductor film with laser light for crystallizing said semiconductor film; treating a surface of the semiconductor film with a hydrofluoric acid after the irradiation of the laser light; and leveling the surface of the crystallized semiconductor film by heating after the treatment with said hydrofluoric acid in an atmosphere, in an atmosphere containing predetermined concentration of oxygen or an oxygen compound (see the English translation Example in Paragraph 0007 through Paragraph 00011).

Although Morosawa discloses irradiating said semiconductor film (i.e., an amorphous silicon film) with a leaser light for crystallizing the semiconductor film, Morosawa is silent about irradiating the semiconductor film with leaser light in air and the concentration of oxygen or oxygen compound being 10 ppm or less.

Kudo et al. disclose method of manufacturing thin film transistor the method includes depositing an amorphous silicon film (25) (i.e., a semiconductor layer) and irradiating the amorphous silicon film (25) with an excimer laser in atmosphere containing an air in order to dehydrogenate the amorphous silicon film and change into polysilicon thin film (see Abstract and Drawing 2).

Both Morosawa and Kudo et al. teachings directed to irradiating amorphous thin film layer using laser light to crystallize the thin film after the thin film deposited for fabrication of TFTs. Therefore, the teachings of Morosawa and Kudo et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with irradiating on the semiconductor film (i.e., amorphous silicon film) in air as taught by Kudo et al. in order to dehydrogenate the amorphous silicon film and convert it to polysilicon thin film.

However, both Morosawa and Kudo et al. do not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Morosawa, Kudo et al. and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al. and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Kudo et al. reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

However, the combination of Morosawa, Kudo et al. and Hara et al. is silent about the concentration of oxygen of oxygen compound being 10 ppm or less during the leveling step.

Although the concentration is not specifically disclosed by Morosawa and Kudo et al., such oxygen concentration rage can be set within the level ordinary skill in the art by routine optimization to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

One of ordinary skill in would have motivated to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed concentration range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 11, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate;

irradiating said semiconductor film with laser light for crystallizing said semiconductor film; treating a surface of the semiconductor film with a hydrofluoric acid after the irradiation of the laser light; and leveling the surface of the semiconductor film by heating after the treatment with said hydrofluoric acid in a reducing atmosphere, in an atmosphere containing predetermined concentration of oxygen or an oxygen compound (see the English translation Example in Paragraph 0007 through Paragraph 00011).

Although Morosawa discloses irradiating said semiconductor film (i.e., an amorphous silicon film) with a leaser light for crystallizing the semiconductor film, Morosawa is silent about irradiating the semiconductor film with leaser light in air and the concentration of oxygen or oxygen compound being 10 ppm or less.

Kudo et al. disclose method of manufacturing thin film transistor the method includes depositing an amorphous silicon film (25) (i.e., a semiconductor layer) and irradiating the amorphous silicon film (25) with an excimer laser in atmosphere containing an air in order to dehydrogenate the amorphous silicon film and change into polysilicon thin film (see Abstract and Drawing 2).

Both Morosawa and Kudo et al. teachings directed to irradiating amorphous thin film layer using laser light to crystallize the thin film after the thin film deposited for fabrication of TFTs. Therefore, the teachings of Morosawa and Kudo et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with irradiating on the semiconductor film (i.e., amorphous silicon film) in air as taught by Kudo et al. in order to dehydrogenate the amorphous silicon film and convert it to polysilicon thin film.

However, both Morosawa and Kudo et al. do not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Morosawa, Kudo et al. and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al. and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Kudo et al. reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

However, the combination of Morosawa, Kudo et al. and Hara et al. is silent about the concentration of oxygen of oxygen compound being 10 ppm or less during the leveling step. Although the concentration is not specifically disclosed by Morosawa and Kudo et al., such oxygen concentration rage can be set within the level ordinary skill in the art by routine optimization to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

One of ordinary skill in would have motivated to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed concentration range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 12, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon over a substrate; irradiating the semiconductor film with laser light for crystallizing said semiconductor film; treating a surface of the semiconductor film with a hydrofluoric acid after the irradiation of the laser light; and leveling the surface of the crystallized semiconductor film by heating after the treatment with the hydrofluoric acid in an inert gas, in an atmosphere containing predetermined

concentration of oxygen or an oxygen compound (see the English translation Example in Paragraph 0007 through Paragraph 00011).

Although Morosawa discloses irradiating said semiconductor film (i.e., an amorphous silicon film) with a leaser light for crystallizing the semiconductor film, Morosawa is silent about irradiating the semiconductor film with leaser light in air and the concentration of oxygen or oxygen compound being 10 ppm or less.

Kudo et al. disclose method of manufacturing thin film transistor the method includes depositing an amorphous silicon film (25) (i.e., a semiconductor layer) and irradiating the amorphous silicon film (25) with an excimer laser in atmosphere containing an air in order to dehydrogenate the amorphous silicon film and change into polysilicon thin film (see Abstract and Drawing 2).

Both Morosawa and Kudo et al. teachings directed to irradiating amorphous thin film layer using laser light to crystallize the thin film after the thin film deposited for fabrication of TFTs. Therefore, the teachings of Morosawa and Kudo et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with irradiating on the semiconductor film (i.e., amorphous silicon film) in air as taught by Kudo et al. in order to dehydrogenate the amorphous silicon film and convert it to polysilicon thin film.

However, both Morosawa and Kudo et al. do not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and

recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Morosawa, Kudo et al. and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al. and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Kudo et al. reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

However, the combination of Morosawa, Kudo et al. and Hara et al. is silent about the concentration of oxygen of oxygen compound being 10 ppm or less during the leveling step. Although the concentration is not specifically disclosed by Morosawa and Kudo et al., such oxygen concentration rage can be set within the level ordinary skill in the art by routine optimization to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

One of ordinary skill in would have motivated to set the oxygen concentration at 10 ppm or less by routine optimization in order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to set the oxygen concentration at 10 ppm or less by routine optimization in

order to passivate the damaged surface of the semiconductor layer during removal of natural (native) oxide, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed concentration range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 14, as applied to claims 1-12 above, both Morosawa , Kudo et al. and Hara et al. in combination discloses all the claimed limitations including leveling (i.e., annealing) the semiconductor film at temperature between 500 and 600 °C (i.e., outside the claimed temperature range of 900 and 1200 °C) (see the English translation Examples in Paragraph 0010).

One of ordinary skill in the art would have been motivated to optimize the claimed annealing temperature range by using routine experimentation in order to achieve the desired device performance.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the claimed annealing temperature range, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d

454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed temperature range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claims 59, 62, 63 and 64, Morosawa discloses a method of manufacturing a semiconductor device comprising the steps of: forming a semiconductor film comprising silicon (2 or 3) (see Drawing 1 and Examples and Abstract) over a substrate (1); irradiating the semiconductor film with laser light for crystallizing the semiconductor film (see Examples Paragraph 0009); removing a natural oxidation film (8) (see Drawing 7 and 8; Examples, Paragraph 0010) formed on a surface of the semiconductor film by etching after the irradiation of the laser light (i.e., by dipping in HF); and leveling the surface of the crystallized semiconductor film with atmosphere containing an inert gas (i.e., N_2) and reducing atmosphere (i.e., H_2) by heating after removing the natural oxidation film; forming a gate insulating layer over the crystallized semiconductor film after the leveling step; and forming an impurity regions in the crystallized semiconductor film after the gate insulating film (i.e., during the S/D contact formation) (see the English translation that was submitted by Applicants on April 18, 2005).

Although Morosawa discloses irradiating said semiconductor film (i.e., an amorphous silicon film) with a leaser light for crystallizing the semiconductor film, Morosawa is silent about irradiating the semiconductor film with leaser light in air.

Kudo et al. disclose method of manufacturing thin film transistor the method includes depositing an amorphous silicon film (25) (i.e., a semiconductor layer) and irradiating the amorphous silicon film (25) with an excimer laser in atmosphere containing an air in order to dehydrogenate the amorphous silicon film and change into polysilicon thin film (see Abstract and Drawing 2).

Both Morosawa and Kudo et al. teachings directed to irradiating amorphous thin film layer using laser light to crystallize the thin film after the thin film deposited for fabrication of TFTs. Therefore, the teachings of Morosawa and Kudo et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa reference with irradiating on the semiconductor film (i.e., amorphous silicon film) in air as taught by Kudo et al. in order to dehydrogenate the amorphous silicon film and convert it to polysilicon thin film.

However, both Morosawa and Kudo et al. do not specifically disclose recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process.

Hara et al. disclose process for fabricating of the thin film semiconductor device (i.e., TFT device) and depositing of the semiconductor layer (2) (i.e., a amorphous silicon layer) and crystallizing of the semiconductor layer (2) and cleaning the semiconductor layer and recrystallizing the semiconductor layer (see Col. 1, line 65 – Col. 2, line 49) in order to level the surface of the semiconductor layer having good uniformity and high reliability (see Hara et al. Figs. 5A-22 and Col. 1, line 65 – Col. 16, line 67).

Morosawa, Kudo et al. and Hara et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al. and Hara et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa and Kudo et al. reference with recrystallizing the semiconductor film in order to level the semiconductor film after native oxide removal process as taught by Hara et al. in order to form a fine semiconductor layer having good uniformity and high reliability.

Re claim 61, as applied to claim 59 above, both Morosawa , Kudo et al. and Hara et al. in combination discloses all the claimed limitations including leveling (i.e., annealing) the semiconductor film at temperature between 500 and 600 °C (i.e., outside the claimed temperature range of 900 and 1200 °C) (see the English translation Examples in Paragraph 0010).

One of ordinary skill in the art would have been motivated to optimize the claimed annealing temperature range by using routine experimentation in order to achieve the desired device performance.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the claimed annealing temperature range, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056

(Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed temperature range or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

8. Claims 13 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Morosawa (JP/07038113), Kudo et al. (JP/09186336) and Hara et al. (US/5,648,276), as applied in claims 1-12 and 15-17 above, and further in view of Yamazaki et al. (US/5,608,232).

The rejection that was mailed on June 26, 2006 is maintained and repeated herein below as of record.

Re claims 13 and 60, as applied to claims 1-12 and 59 respectively in Paragraph 7 above, Morosawa, Kudo et al. and Hara et al. in combination disclose all the claimed limitations including annealing of the substrate during the leveling step.

However, the combination of Morosawa, Kudo et al. and Hara et al. do not specifically disclose furnace annealing.

Yamazaki et al. disclose furnace annealing of the substrate in nitrogen atmosphere in order to crystallize the semiconductor layer (see Yamazaki et al. Col. 24, lines 10-30).

Morosawa, Kudo et al., Hara et al. and Yamazaki et al. teachings are directed to fabricating of TFTs the process includes depositing of semiconductor thin film and annealing the semiconductor thin film the crystallize the thin film. Therefore, the teachings of Morosawa, Kudo et al., Hara et al. and Yamazaki et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Morosawa, Kudo et al. and Hara et al. reference with furnace annealing during leveling process of the semiconductor layer as taught by Yamazaki et al. in order to crystallize the semiconductor layer.

Response to Arguments

9. Applicants' arguments filed September 29, 2006 have been fully considered but they are not persuasive.

Applicants argue that "the vacuum of Morosawa does not correspond with an atmosphere containing oxygen as recited in claims 19, 20, 47 and 48. Therefore, Morosawa does not teach or suggest irradiating a semiconductor film with laser light in an atmosphere containing oxygen for crystallizing the semiconductor film.

In response to applicants' argument, it is respectfully submitted that the prior art of record in combination disclose all the claimed limitation including "irradiating the semiconductor film in atmosphere containing oxygen."

Morosawa clearly discloses crystallizing of the amorphous silicon layer in order to form a polycrystalline silicon layer and also clearly disclose removal of native oxide film after laser anneal crystallization process. The presence of the native oxide film provides an evidence there existence of oxygen in the chamber at any form. Therefore, the prior art meets the limitation of "irradiating of the semiconductor film with laser light *atmosphere containing oxygen.*" In addition, applicants do not specifically claimed in what form oxygen gas presented in the chamber during laser annealing process. Since applicants' do not specifically claimed particular form oxygen presence in the chamber, such as, oxygen gas supplied into the chamber, moisture containing oxygen, or air present in the camber, the formation of the native oxide layer provides

an inherent presence of oxygen or oxygen containing ambient in the chamber of the prior art of Morosawa disclosure.

Claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Morosawa clearly discloses crystallizing of the amorphous silicon layer in order to form a polycrystalline silicon layer (i.e., crystalline semiconductor layer) prior removing the native oxide and leveling surface. Further process that performed with regarding of leveling process which re-recrystallization of the semiconductor layer is done on previously crystallized semiconductor layer. The difference between the Morosawa and the instant application claimed invention is that the instant application is claimed *recrystallizing the previously crystallized semiconductor film in order to level the semiconductor film after native oxide removal process.* While Morosawa is silent about the *recrystallizing the crystallized semiconductor film,* Morosawa discloses *removing of the native oxide layer* form the *previously crystallized semiconductor film* by cleaning. The prior art of record that used to rejected the instant application directed to fabricating of TFTs and the process includes depositing of semiconductor thin film and annealing the semiconductor thin film to crystallize the thin film. Therefore, the teachings of the prior art of record are analogous. One having ordinary skill in the are would have expected reasonable success by improving the surface uniformity of the crystalline silicon layer as suggested by Hara et al. by forming fine semiconductor layer having good uniformity and high reliability. In addition, one having ordinary skill in the art would have been motivated

to look to analogous art teaching suitable or useful methods for performing recrystallizing the semiconductor film in order to produce a semiconductor device having semiconductor thin film with good uniformity and high reliability because such process is recognized by Hara et al. for its suitability of an intended purpose.

Further in response to applicants' argument with disagreeing with the motivation to combine the Hara reference, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Finally, it is respectfully submitted that the first excimer laser heating in the Morsawa reference converts the amorphous silicon to polycrystalline silicon. However, during the HF treatment, the silicon film crystal structure will be damaged and the Hara's melting recrystallization step helps improve film quality of the silicon layer. The motivation directly can be found in the Hara et al. reference because such process will improve uniformity and high reliability the silicon film. Therefore, the combination is proper.

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Applicants' submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on October 20, 2006 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brook Kebede

Brook Kebede
Primary Examiner
Art Unit 2823

BK
December 11, 2006